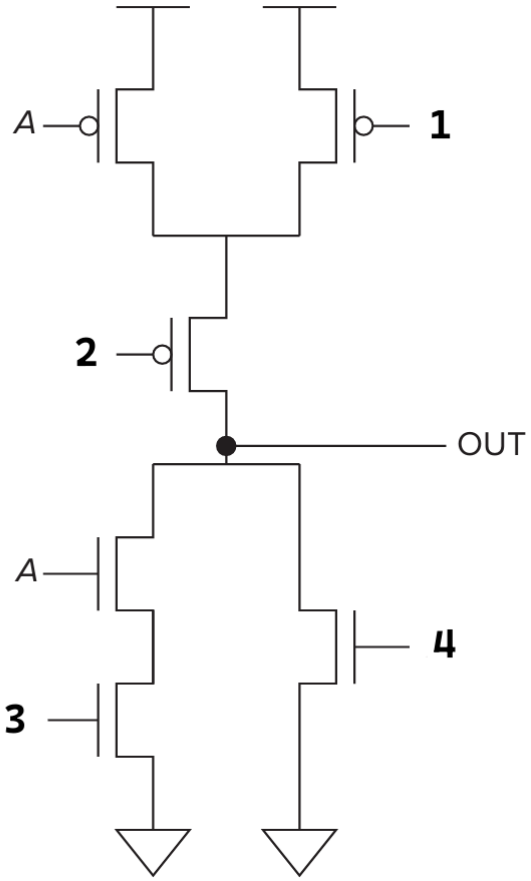
HW 2

T1

Prove that the NAND gate, by itself, is logically complete (see Section 3.3.5) by constructing a logic circuit that performs the AND function, a logic circuit that performs the NOT function, and a logic circuit that performs the OR function. Use only NAND gates in these three logic circuits.

T2

Transistor circuit shown below produces the accompanying truth table. The inputs to some of the gates of the transistors are not specified. Also, the outputs for some of the input combinations of the truth table are not specified. Complete both specifications. i.e., all transistors will have their gates properly labeled with either A, B, or C, and all rows of the truth table will have a 0 or 1 specified as the output.



A	B	C	OUT
0	0	0	
0	0	1	0
0	1	0	
0	1	1	
1	0	0	1
1	0	1	
1	1	0	
1	1	1	

T3

Shown below are several logical identities with one item missing in each. X represents the case where it can be replaced by either a 0 or a 1 and the identity will still hold. Your job: Fill in the blanks with either a 0, 1, or X. For example, in part a, the missing item is X. That is 0 OR 0 = 0 and 0 OR 1 = 1.

- 0 OR X = __
- 1 OR X = __
- 0 AND X = __
- 1 AND X = __
- __ XOR X = X

T4

Design a XNOR gate with NAND gates.

A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

T5

1. For the memory shown in Figure 3.45:

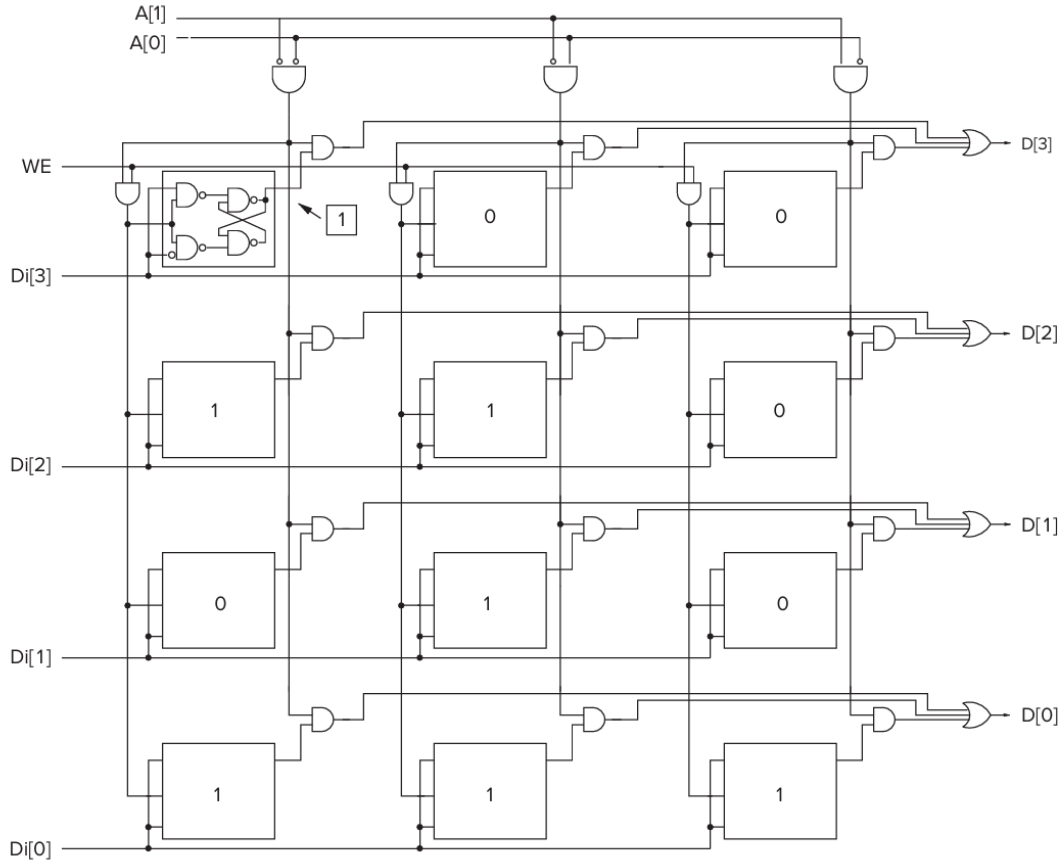


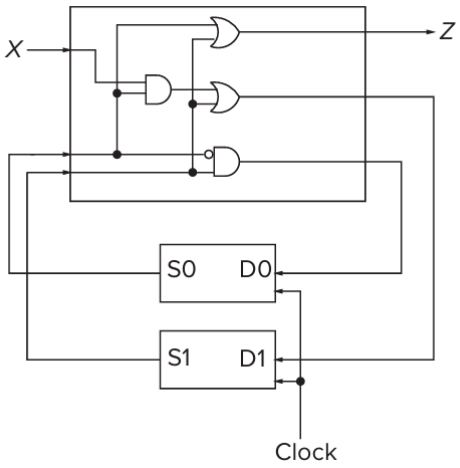
Figure 3.45 Diagram for Exercise 3.40.

- What is the address space?
- What is the addressability?
- What is the data at address 1?

2. If a computer has eight-byte addressability and needs four bits to access a location in memory, what is the total size of memory in bytes?

T6

The following figure shows an implementation of a finite state machine with an input X and output Z. S1, S0 specifies the present state. D1, D0 specifies the next state.



1. Complete the following table.

S1	S0	X	D1	D0	Z
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

2. Draw the state diagram for the truth table of part 1.

T7

Suppose a 32-bit instruction takes the following format:

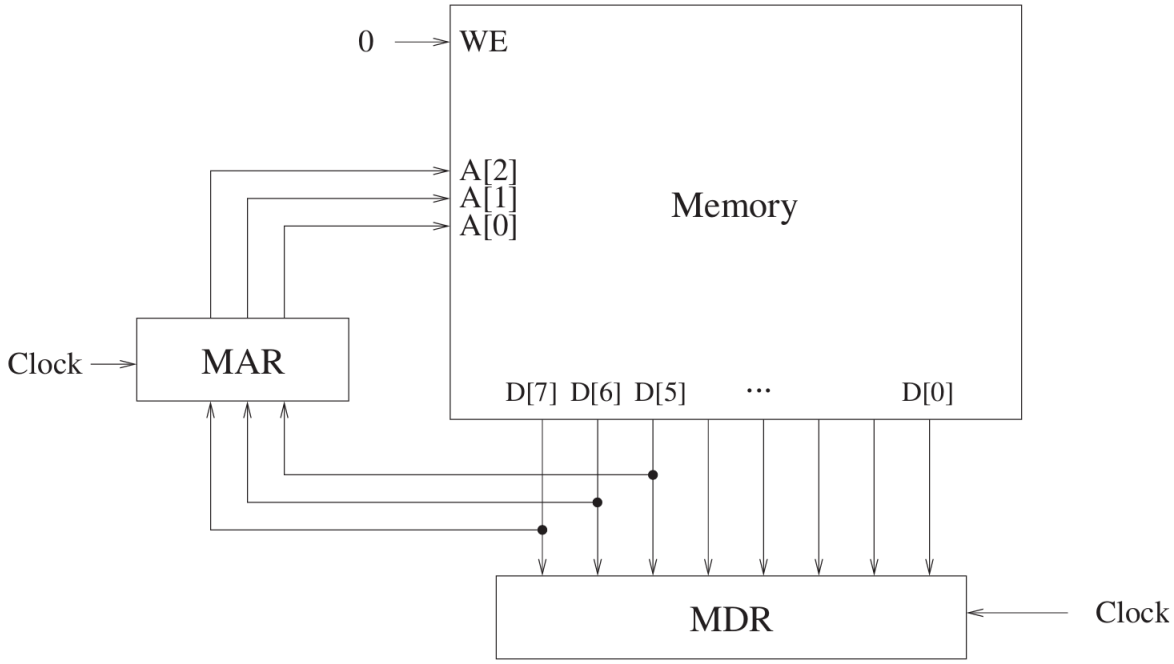
If there are 56 opcodes and 40 registers, what is the range of values that can be represented by the immediate (IMM)? Assume IMM is a 2's complement value.

T8

Say it takes 50 cycles to read from or write to memory and only one cycle to read from or write to a register. Calculate the number of cycles it takes for each phase of the instruction cycle for both the IA-32 instruction "ADD [eax], edx" (refer to) and the LC-3 instruction "ADD R6, R2, R6." Assume each phase (if required) takes one cycle, unless a memory access is required.

T9

Shown below is a byte-addressible memory consisting of eight locations, and its associated MAR and MDR. Both MAR and MDR consist of flip-flops that are latched at the start of each clock cycle based on the values on their corresponding input lines. A memory read is initiated every cycle, and the data is available by the end of that cycle.



Just before the start of cycle 1, MAR contains 000, MDR contains 00010101, and the contents of each memory location is as shown.

Memory Location	Value
x0	01010000
x1	11110001
x2	10000011
x3	00010101
x4	11000110
x5	10101011
x6	00111001
x7	01100010

1. What do MAR and MDR contain just before the end of cycle 1?
2. What does MDR contain just before the end of cycle 4?